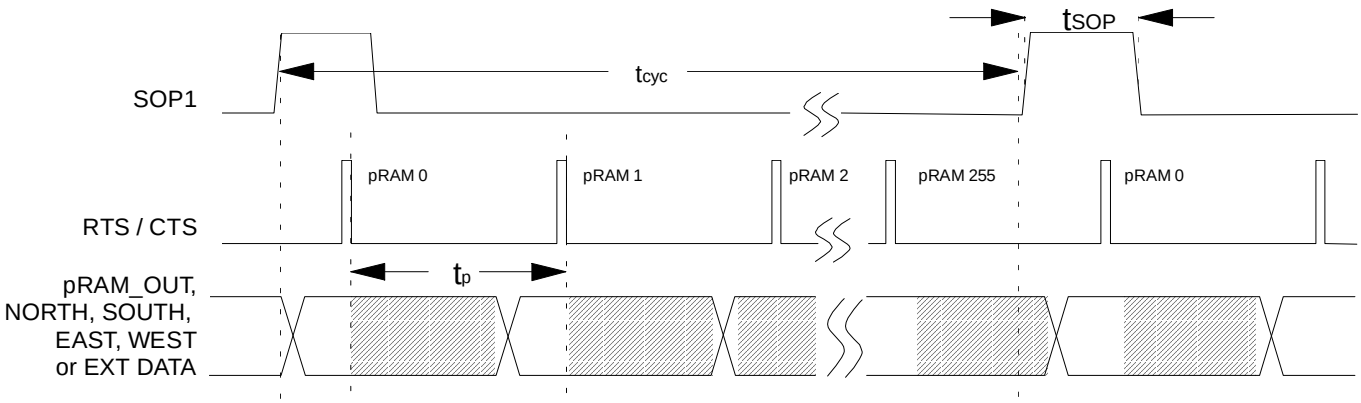
pRAM-256 TIMING

$_{CLK}$	input clock rate	33MHz maximum (determined by t_{AC} of SRAM)	
t_{AC}	access time of external SRAM	25 nS	
t_{cyc}	pRAM-256 cycle time (training disabled)	0.154 mS	(5120 cycles of CLK @ 33MHz)
t_{cycL}	pRAM-256 cycle time (training enabled)	0.246 mS	(8192 cycles of CLK @ 33MHz)
t_{p}	interval between pRAM outputs	600ns	(20 cycles of CLK @ 33 MHz)
t_{SOP}	SOP1 pulse width	600ns	(20 cycles of CLK @ 33 MHz)
t_{WE}	WE pulse width	40ns minimum	
t_{SRAM}	SRAM cycle time	60ns	(2 cycles of CLK @ 33MHz)
t_{RRW}	RRW pulse width	40ns minimum	
t_{RTS}	RTS pulse width	40ns minimum	

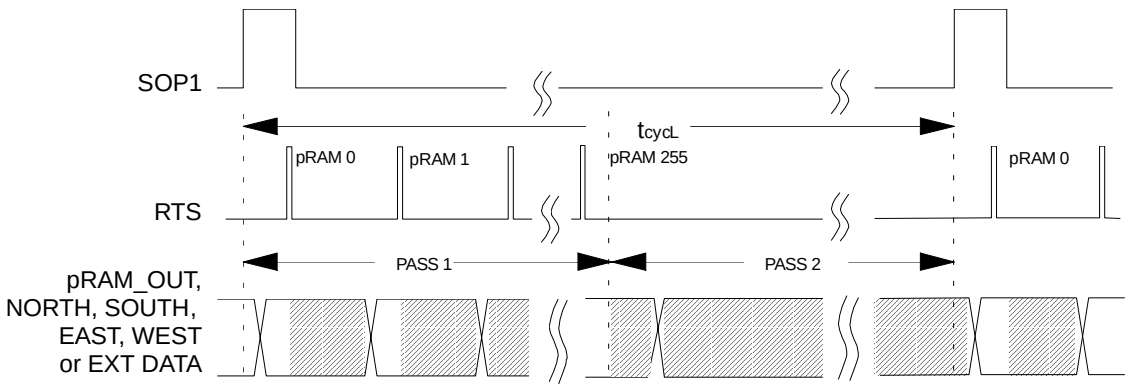
INPUT AND OUTPUT DATA
NO TRAINING



NOTES:
ACK_HALT = 0
ACK_TRAIN = 0

DATA IS LATCHED INTO ON-CHIP MEMORY ON THE TRAILING EDGE OF CTS

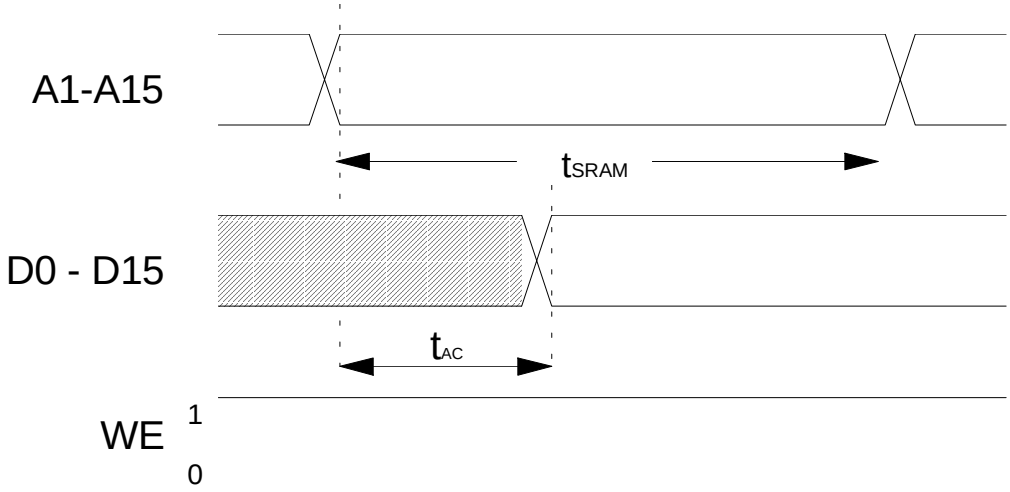
WITH TRAINING ENABLED



NOTES:
ACK_HALT = 0
ACK_TRAIN = 1

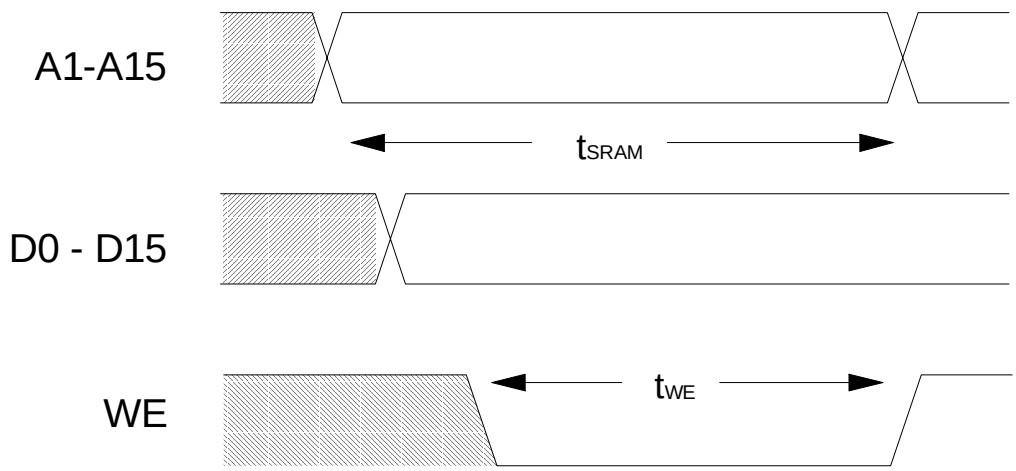
DATA IS TRANSFERRED DURING PASS 1 ONLY

READ CYCLE



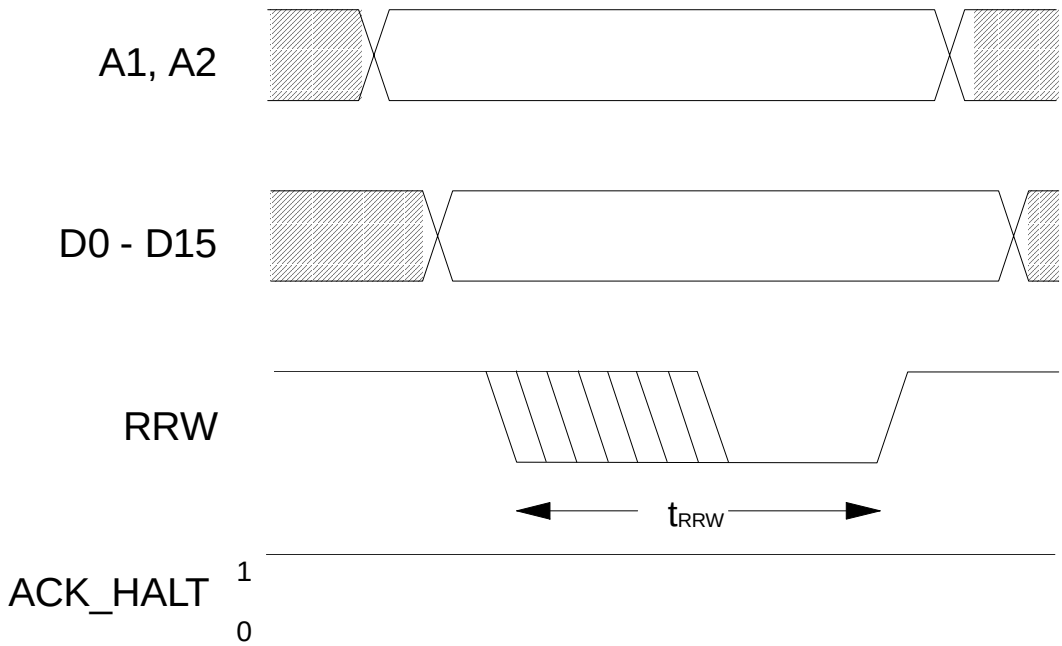
NOTE:
ACK_HALT = 0

WRITE CYCLE



NOTE:
ACK_HALT = 0

WRITE TO pRAM-256 INTERNAL REGISTERS



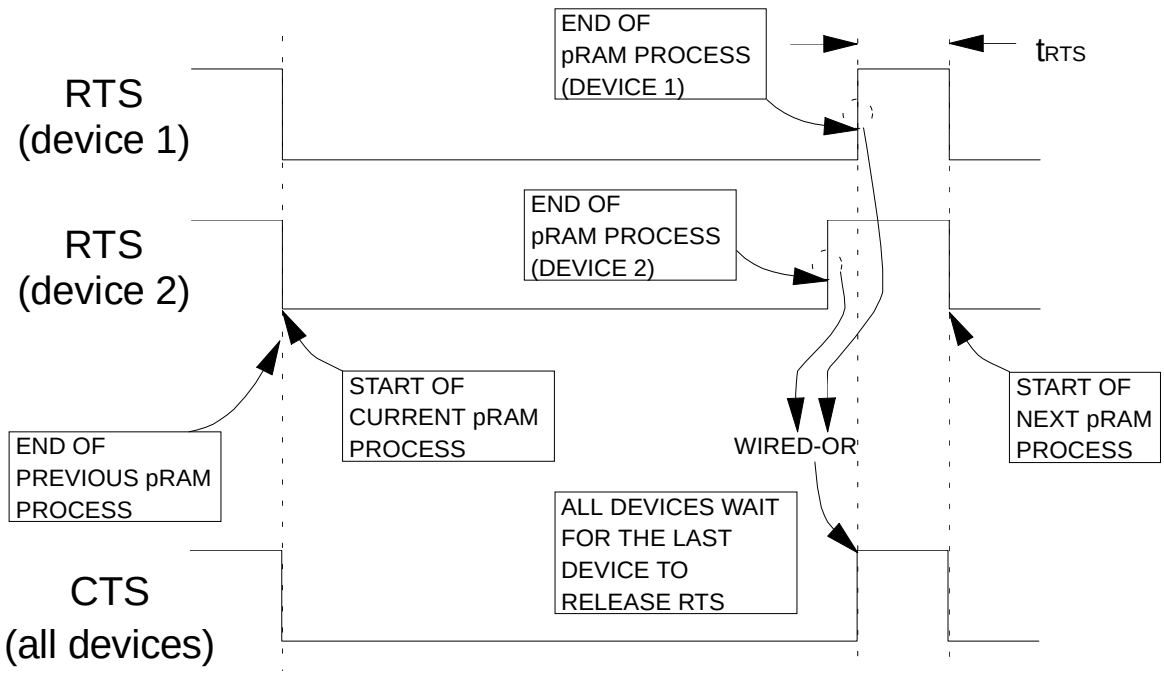
NOTE 1:
ACK_HALT INDICATES THAT A1, A2 and D0-D15 ARE TRI-STATED. EXTERNAL CIRCUITRY MUST WAIT FOR ACK_HALT TO BE ASSERTED BEFORE ATTEMPTING TO USE THE BUSES.

NOTE 2:
AFTER ACK_HALT GOES HIGH, RRW SHOULD NOT BE IN A LOW STATE WHEN A1 OR A2 ARE CHANGING AS THE CONDITION A1=0 A2=1 WILL CAUSE THE FEEDBACK POLYNOMIAL REGISTER TO BE CORRUPTED

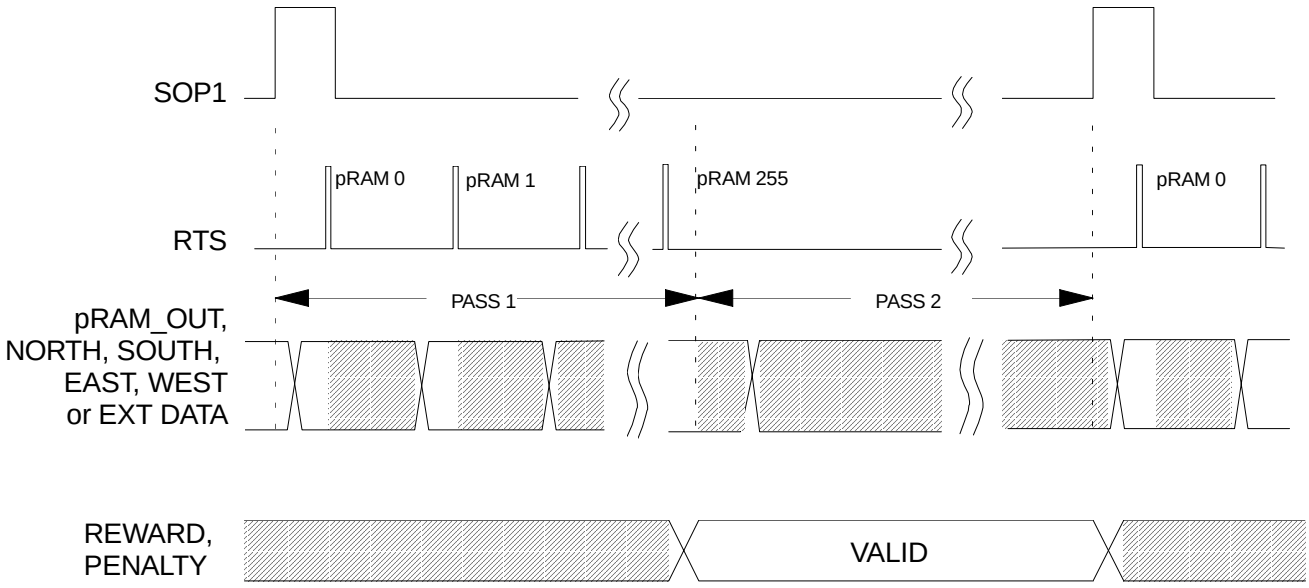
MULTIPLE pRAM-256 ARRAYS

SYNCHRONISATION BETWEEN pRAM-256 MODULES IS MAINTAINED BY WIRING TOGETHER THE OPEN-DRAIN OUTPUTS (RTS) AND CONNECTING THE RESULTING SIGNAL TO THE CTS INPUT OF ALL DEVICES.

THIS ENSURES THAT THE EXCHANGE OF DATA BETWEEN pRAM-256 MODULES ONLY OCCURS WHEN THE pRAM_OUT DATA OF ALL MODULES IS VALID.



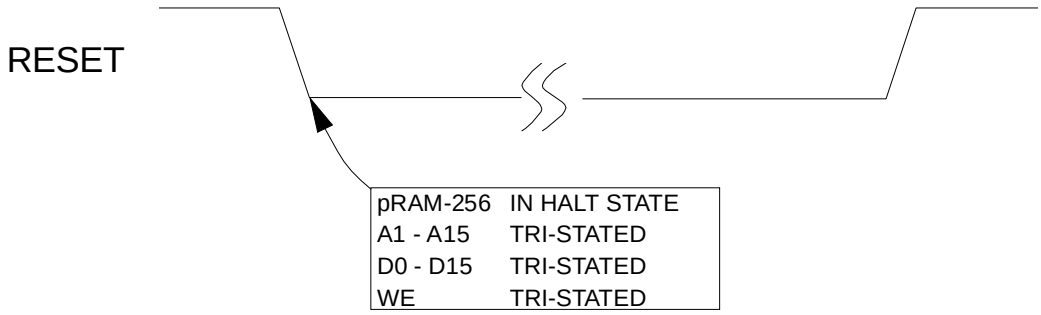
REWARD AND PENALTY INPUTS



NOTES:
ACK_HALT = 0 , ACK_TRAIN = 1

REWARD & PENALTY ARE NOT LATCHED INTERNALLY TO THE pRAM-256. THESE SIGNALS SHOULD BE LATCHED EXTERNALLY DURING PASS 2 OF THE pRAM-256. SOP1 MAY BE USED AS A STROBE TO LATCH THE REWARD AND PENALTY SIGNALS.

RESET



NOTE:
RESET SETS THE INTERNAL FEEDBACK POLYNOMIAL GENERATOR TO ITS INITIAL STATE AND RESETS ALL INTERNAL COUNTERS SO THAT PROCESSING OF pRAM #0 STARTS AS SOON AS RESET GOES HIGH.